L Number	Hits	Search Text	DB'	Time stamp
1	959869	TAP interface with STP interface	USPAT;	2004/02/18 10:33
			US-PGPUB;	200 , 0 = , = 0 = 0.00
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
2	821654	TAP/STP interface\$1	USPAT;	2004/02/18 10:33
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
3	812532	(TAP interface with STP interface) and (TAP/STP interface\$1)	USPAT;	2004/02/18 10:33
			US-PGPUB;	
			EPO; JPO;	ļ
			DERWENT;	
4	925	"IEEE 1149.1"	IBM_TDB	2004/02/10 10:22
7	925	1000 1149.1	USPAT;	2004/02/18 10:33
			US-PGPUB;	
			EPO; JPO; DERWENT;	
			IBM_TDB	
5	748	((TAP interface with STP interface) and (TAP/STP interface\$1))	USPAT;	2004/02/18 10:34
"	/ .0	and "IEEE 1149.1"	US-PGPUB;	2004/02/10 10.54
		410 1222 1711	EPO; JPO;	
			DERWENT;	
			IBM_TDB	
6	3789571	integrated circuit	USPAT;	2004/02/18 10:34
			US-PGPUB;	200 1, 02, 10 10.5 1
İ			EPO; JPO;	
			DERWENT;	
		10	IBM_TDB	
7	721	(((TAP interface with STP interface) and (TAP/STP interface\$1))	USPAT;	2004/02/18 10:37
		and "IEEE 1149.1") and (integrated circuit)	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	4600705		IBM_TDB	
8	4699725	single mode test access port\$1	USPAT;	2004/02/18 10:37
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
9	3557090	dual mode test access port\$1	IBM_TDB	2004/02/19 10:27
	3337030	dudi mode test access port#1	USPAT; US-PGPUB;	2004/02/18 10:37
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
10	721	(((((TAP interface with STP interface) and (TAP/STP interface\$1))	USPAT;	2004/02/18 10:47
		and "IEEE 1149.1") and (integrated circuit)) and ((single mode	US-PGPUB;	
		test access port\$1) with (dual mode test access port\$1))	EPO; JPO;	
			DERWENT;	
			IBM_TDB	
11	3673415	TAP clock circuit	USPAT;	2004/02/18 10:48
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
12	2000040	deba marketanda	IBM_TDB	
12	3009849	data register\$1	USPAT;	2004/02/18 10:49
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	1
L			IBM_TDB	

13	715	(((((TAP interface with STP interface) and (TAP/STP interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port\$1) with (dual mode test access port\$1))) and (data register\$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/02/18 10:49
		(IBM_TDB	
14	881110	instruction register	USPAT; US-PGPUB; EPO; JPO;	2004/02/18 10:49
			DERWENT;	
15	604	/////TAD interference with CTD interference and /TAD/CTD interference	IBM_TDB	2004/02/40 40 40
15	694	((((((TAP interface with STP interface) and (TAP/STP interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode	USPAT; US-PGPUB;	2004/02/18 10:49
		test access port\$1) with (dual mode test access port\$1))) and	EPO; JPO;	
		(data register\$1)) and (instruction register)	DERWENT;	
16	664	((((((TAP interface with STP interface) and (TAP/STP	IBM_TDB USPAT;	2004/02/18 10:50
10		interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	US-PGPUB;	2004/02/16 10.50
		((single mode test access port\$1) with (dual mode test access	EPO; JPO;	
		port\$1))) and (data register\$1)) and (instruction register)) and (TAP clock circuit)	DERWENT; IBM_TDB	
17	130773	multiplexer\$1	USPAT;	2004/02/18 10:50
			US-PGPUB;	=====================================
			EPO; JPO; DERWENT;	
			IBM_TDB	
18	407	(((((((TAP interface with STP interface) and (TAP/STP	USPAT;	2004/02/18 10:51
		interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	US-PGPUB;	
		((single mode test access port\$1) with (dual mode test access port\$1))) and (data register\$1)) and (instruction register)) and	EPO; JPO; DERWENT;	
		(TAP clock circuit)) and multiplexer\$1	IBM_TDB	
19	1257443	TAP controller	USPAT;	2004/02/18 10:51
			US-PGPUB; EPO; JPO;	
			DERWENT;	
20	358	(((((((TAD into force with CTD into force) and (TAD (CTD	IBM_TDB	2004/02/40 40 54
20	336	((((((((TAP interface with STP interface) and (TAP/STP interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	USPAT; US-PGPUB;	2004/02/18 10:51
		((single mode test access port\$1) with (dual mode test access	EPO; JPO;	
		port\$1))) and (data register\$1)) and (instruction register)) and	DERWENT;	
21	2219415	(TAP clock circuit)) and multiplexer\$1) and (TAP controller) scan test port	IBM_TDB USPAT;	2004/02/18 10:52
			US-PGPUB;	200 1/02/10 10:32
			EPO; JPO;	
			DERWENT; IBM_TDB	
22	357	((((((((TAP interface with STP interface) and (TAP/STP	USPAT;	2004/02/18 10:55
		interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and ((single mode test access port\$1) with (dual mode test access	US-PGPUB;	
		port\$1))) and (data register\$1)) and (instruction register)) and	EPO; JPO; DERWENT;	
		(TAP clock circuit)) and multiplexer\$1) and (TAP controller)) and	IBM_TDB	
23	1704259	(scan test port) scan path	USPAT;	2004/02/40 40:55
23	1704239	Scarr paul	US-PGPUB;	2004/02/18 10:55
			EPO; JPO;	
			DERWENT;	
24	354	((((((((TAP interface with STP interface) and (TAP/STP	IBM_TDB USPAT;	2004/02/18 10:55
		interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	US-PGPUB;	, _ , _ , ,
		((single mode test access port\$1) with (dual mode test access port\$1))) and (data register\$1)) and (instruction register)) and	EPO; JPO;	
		(TAP clock circuit)) and multiplexer\$1) and (TAP controller)) and	DERWENT; IBM_TDB	
		(scan test port)) and (scan path)		

	1			T
25	871331	core\$1	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/02/18 10:55
26	203	((((((((((((((((((((((((((((((((((((((IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:56
27	822348	(scan test port)) and (scan path)) and core\$1 scan register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:57
28	203	((((((((((((((((((((((((((((((((((((((USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:58
29	139253	accessing and (data register with first access protocol)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:59
30	125	((((((((((((((((((((((((((((((((((((((USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:59
31	139247	accessing and (data register with second access protocol)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 10:59
32	125	((((((((((((((((((((((((((((((((((((((USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:00
33	1560115	test instruction	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:01
34	125	((((((((((((((((((((((((((((((((((((((USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:01

35	544856	in-circuit emulation register	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/02/18 11:01
36	544857	((((((((((((((((((((((((((((((((((((((IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:01
37	669813	(test instruction)) afnd (in-circuit emulation register) in-circuit programming register	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2004/02/18 11:01
38	537545	((((((((((((((((((((((((((((((((((((((IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:02
39	1123557	boundary scan register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:02
40	683998	bypass register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:03
41	545759	(boundary scan register) and (bypass register)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:03
42	534086	((((((((((((((((((((((((((((((((((((((USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:05
43	5468563	select\$4 dual mode test access port	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/18 11:05

44	338696	((((((((((((((((((((((((((((((((((((((USPAT;	2004/02/18 11:06
		interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	US-PGPUB;	, ,
		((single mode test access port\$1) with (dual mode test access	EPO; JPO;	
		port\$1))) and (data register\$1)) and (instruction register)) and	DERWENT;	
		(TAP clock circuit)) and multiplexer\$1) and (TAP controller)) and	IBM_TDB	
		(scan test port)) and (scan path)) and core\$1) and (scan register))		
		and (accessing and (data register with first access protocol))) and		
		(accessing and (data register with second access protocol))) and		
		(test instruction)) afnd (in-circuit emulation register)) and		
		(in-circuit programming register)) and ((boundary scan register)		
		and (bypass register))) and (select\$4 dual mode test access port)		
45	5009	714/724.ccls. or 714/725.ccls. or 714/727.ccls. or 714/733.ccls. or	USPAT;	2004/02/18 11:08
		714/734.ccls. or 714/30.ccls. or 714/726.ccls.	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	2024		IBM_TDB	
46	2324	((((((((((((((((((((((((((((((((((((((USPAT;	2004/02/18 11:09
		interface\$1)) and "IEEE 1149.1") and (integrated circuit)) and	US-PGPUB;	
		((single mode test access port\$1) with (dual mode test access	EPO; JPO;	
		port\$1))) and (data register\$1)) and (instruction register)) and	DERWENT;	
		(TAP clock circuit)) and multiplexer\$1) and (TAP controller)) and	IBM_TDB	
		(scan test port)) and (scan path)) and core\$1) and (scan register))		
		and (accessing and (data register with first access protocol))) and		
		(accessing and (data register with second access protocol))) and		
		(test instruction)) afnd (in-circuit emulation register)) and		
		(in-circuit programming register)) and ((boundary scan register) and (bypass register))) and (select\$4 dual mode test access port))		
		and (714/724.ccls. or 714/725.ccls. or 714/727.ccls. or		
		714/733.cds. or 714/734.ccls. or 714/30.cds. or 714/726.ccls.)		
47	107	714/729.ccls.	USPAT;	2004/02/18 11:09
.,	107	721/723.003.	US-PGPUB;	2004/02/10 11:09
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
48	60	((((((((((((((((((((((((((((((((((((((USPAT;	2004/02/18 11:09
		(TAP/STP interface\$1)) and "IEEE 1149.1") and (integrated	US-PGPUB;	200 1, 02, 10 11.05
		circuit)) and ((single mode test access port\$1) with (dual mode	EPO; JPO;	
		test access port\$1))) and (data register\$1)) and (instruction	DERWENT;	
		register)) and (TAP clock circuit)) and multiplexer\$1) and (TAP	IBM_TDB	
		controller)) and (scan test port)) and (scan path)) and core\$1)	_	
		and (scan register)) and (accessing and (data register with first		
		access protocol))) and (accessing and (data register with second		
		access protocol))) and (test instruction)) afnd (in-circuit emulation		
		register)) and (in-circuit programming register)) and ((boundary		
		scan register) and (bypass register))) and (select\$4 dual mode		
		test access port)) and (714/724.ccls. or 714/725.ccls. or	-	
		714/727.ccls. or 714/733.ccls. or 714/734.ccls. or 714/30.ccls. or		
		714/726.ccls.)) and 714/729.ccls.		